

1 ABSTRACT

2 A memory controller for a wireless communication system
3 comprises a packet buffer write system and a packet buffer
4 read system. The packet buffer write system places packets
5 including packet header and packet data into a packet
6 buffer. The packet buffer read system removes packets
7 including a packet header and packet data from a packet
8 buffer. The packet buffer is arranged into a plurality of
9 packet buffer memory slots, each slot comprising a
10 descriptor status array location including an availability
11 bit set to "used" or "free", and a packet buffer memory
12 location comprising a descriptor memory slot and a data
13 segment memory slot. The descriptor memory slot includes
14 header information for each packet, and the data segment
15 memory slot includes packet data. The memory controller
16 operates on one or more queues of data, and data is placed
17 into a particular queue in packet memory determined by
18 priority information derived from incoming packet header or
19 packet data. Data is removed from packet memory based on
20 which queue the data may be found in. The queues are based
21 on a priority system, where one queue receives priority over
22 another queue for data reception and transmission.